NOTICE INVITING EXPRESSION OF INTEREST

FOR

TRANSFER OF TECHNOLOGY FOR
"HIGH SPEED RECONFIGURABLE POWER ELECTRONIC CONTROLLER (HSRPEC)"

EoI No: NaMPET-III/HSRPEC/EoI/2022

EoI release date: 27/05/2022

Centre for Development of Advanced Computing (CDAC)
Thiruvananthapuram

1. Introduction

National Mission on Power Electronics Technology (NaMPET) is a programme launched bythe Ministry of Electronics and Information Technology (MeitY), Govt. of India in 2004, with a vision to provide the country with capability to become a dominant player in Power Electronics Technology. Through this Programme, Research, Development, Deployment and Commercialization of Power Electronics Technology is envisaged by enhancing the indigenous R&D expertise and infrastructure in the country with active participation from academic institutions and industries. Centre for Development of Advanced Computing (CDAC), Thiruvananthapuram, a premier R&D organization under MeitY, is the Nodal Centre for coordinating the activities of NaMPET. Two phases of this National level program each with 5-year duration has been successfully completed. MeitY initiated the Third phaseof NaMPET (NaMPET Phase-III) in January 2019 for five years aiming further strengtheningof the power electronics technology base in the country, through the second phase of NaMPET a new re-configurable controller design methodology called High Speed Reconfigurable Power Electronic Controller (HSRPEC) was developed and deployed in more than 11 institutions for popularization of the methodology .

2. About High Speed Reconfigurable Power Electronic Controller (HSRPEC)

The increasing use of power electronic converters and electrical drives in both domestic and industrial systems over recent years has led to a rapid development of devices and circuit topologies. At the core of these systems is the control strategy adopted to meet the requirements of application. Conventional designs of industrial Power Electronic controls are based on microcontrollers and Digital signal Processors (DSPs). Microcontrollers change too often and there is lots of re-work required to be done in order to keep pace with changing technology. Traditional digital signal processors are microprocessors designed to perform a specialized purpose. They are well-suited to algorithmic-intensive tasks but are limited in performance by clock rate and the sequential nature of their internal design. Multicore architectures may increase performance, but these are still limited. A solution to the increasing complexity of DSP implementations came with the introduction of FPGA technology which allows hardware re-configurability. They may be programmed using high- level description languages like VHDL and Verilog, or at a block diagram level. FPGAs also have the inherent advantage of product reliability and maintainability.

Hence reconfigurable architectures have proven to provide high performance in a wide range of applications. A soft-core processor is a hardware description language (HDL) model of a specific processor (CPU) that can be customized for a given application and synthesized for an ASIC or FPGA target. As the soft processor is in a configurable format we can add algorithmic intensive modules designed in HDL (like PWM, PI, Clarke and Park Transforms etc.) to the CPU. These modules can be accessed through custom instructions/functions through an application program. Thus, the user is designing a custom processor with his own instructions. This processor shall be downloaded to any FPGA then the FPGA becomes the physical processor. Depending on application the user shall change configurations or modules inside FPGA. The

above said concept is used in HSRPEC.As the algorithmic modules are in hardware the HSRPEC will perform faster than its software implementation in equivalent DSP implementation. Also, HSRPEC uses hardware parallel processing than software pipelining. As the processor design is in soft format which can be downloaded to any FPGA, processor obsolescence risk is minimum in HSRPEC methodology. The use of custom IPs reduces the software overhead, the number of lines in application program is less than its equivalent DSP/Microprocessor design. As we have the proven IP set and FPGA board which shall improve the time to market criteria. In HSRPEC at any point of time the user can shift from single core to multi core design without any change in FPGA board. One can use his own CPU designed in HDL or off the shelf CPU core like CDAC's VEGA, NIOS II etc.

3. Application Areas.

As a generic high performance controller for various power electronics applications like

- High performance drives
- Power converters
- Solar MPPT applications
- Smart metering
- Communication controller(Custom/standard) in Power electronics applications
- Power quality applications
- Education and training

4. Features

- Soft processor integrated re configurable PE controller
- Application specific processor design
- Wide range of PE specific IP libraries
- User defined Instructions
- Reduces software coding overhead
- Explores hardware parallel processing

5. Technology Transfer

The technology will be transferred on non-exclusive basis.

I. Direct offer of Technology (DoT) for Academic Institutions

- Deliverables
  - HSRPEC Controller card V1.1 (1 No)
  - HSRPEC Peripheral Interface card V1.1(1No)
  - 10 Power electronic specific IPs (Only netlists)
  - User manual and application example manual
  - Support for Including and Developing new IPs if needed

DoT fee: Rs. 25,000 (Excluding Taxes)

For Training: Rs. 25,000 (Excluding Taxes) limited to 5 persons for 5 working days at CDAC.

II. Full Technology Transfer (ToT)

- Deliverables
  - HSRPEC Controller card V1.1 (2 No)
  - HSRPEC Peripheral Interface card V1.1(2 No)
  - Gerber and Schematic of the Controller and Peripheral Interface card
  - 10 Power electronic specific IPs with Source code
  - HSRPEC IP design procedure
  - User manual and application example manual
  - 10-man day training at CDAC-T
  - Support for IP deign
  - ToT fee: 7 Lakhs including training

6. General terms and conditions

1. An expert committee constituted by MeitY/C-DAC will scrutinize the applications for follow-up action.
2. The applicants may be called for a presentation regarding their strengths and business proposals
3. All incidental expenditure incurred in preparation/ submission or presentation of theEoI shall be borne by the participating agency
4. Participation in this EoI does not guarantee any association with C-DAC unless notifiedby MeitY/C-DAC in writing.
5. MeitY/C-DAC reserves the right of rejecting any offer without assigning reasons.
6. There is neither a business guarantee nor any commitment for funding support from MeitY/C-DAC to the appointed/ empanelled agencies.
7. A Committee of experts constituted by MeitY/C-DAC will assess capabilities and strengths of the industry before finalizing the technology partners.
8. The industry willing to take technology for commercial production will be required to enter into a ToT agreement with C-DAC as per the terms and conditions approved bythe competent authority in the MeitY in the prescribed format.

7. Eligibility

Companies/organizations with expertise in recreational vessel manufacturing/operating industry, especially in Power electronic and Academic Institutions as per the ToT guideline agreement of C-DAC are eligible to apply. Industries working on in development& deployment of power conversion systems can apply.Professionally managed companies, corporates and startups are also welcome to apply forthe technology.

8. How to apply

Interested companies/industries may send expression of interest with their details by filling the EoI form as per Annexure – I to the following address.

Ajeesh A
Scientist E/Joint Director Power
Electronics Group CDAC
ThiruvananthapuramKerala
PIN: 695033
Ph: 0471-2723333-365 (extn)
Email: a j e e s h @ c d a c . i n

Please follow the below link for product brochure

https://nampet.in/images/technology_available/HSRPEC.pdf

Annexure-I

Details of Expression of Interest

(To be filled by the organization interested in technology transfer from C-DAC(T))

Sl No.	Description of Items	Details from Organisation
1	Name of the Organisation Address of registered office with telephone no. & fax	
2	Contact Details Name Designation Address for Comm. Email & Phone	
3	About Organisation Website if available	
4	Any Additional Technology development request	
5	Readiness level to take the technology	
6	Any other information request	
7	Feedback on the information shared by C-DAC(T)	

Declaration

I/We hereby confirm that I/we are interested in the above technology and would productionise it as per terms and conditions. All the information provided above is genuine and accurate.

Authorized Person's Signature.

Name and Designation:

Date of Signature: