[File no.- 27(14)/2013-IPHW]

**Government of India**

**Ministry of Communication & Information Technology**

**Department of Electronics & Information Technology (DeitY)**

Date : 24 - 05-2013

## ORDER

**Subject: Constitution of Technical Evaluation Committee (MSIPS) for Assembly Testing Marking and Packaging**

Reference: 1. MSIPS Policy Gazette Notification No. 175 dated 27-07-2012
2. MSIPS Guidelines dated 07-10-2012

The Modified Special Incentive Package Scheme ( M-SIPS) to offset disability and attract investment in Electronics System Design and Manufacturing(ESDM) in India was notified vide Notification no. 175 dated 27th July 2012 in Part-I , Section 1 of the Gazette of India (Extraordinary) [File no.- 24(10)/2012-IPHW ]. As per para 6.2 of the notification , for effective functioning of M-SIPS a set of guidelines dated 07-10-2013 have been drawn and issued by the Department. [ File no. 27(3)/2012-IPHW].

2. In furtherance of para 8 of the above cited guidelines , Technical Evaluation Committees for following activities is constituted:

**"Assembly Testing Marking and Packaging ( ATMP) of Logic Microprocessor, Memory, Chip Components, Discrete Semiconductors, Power Semiconductors, LEDs, LCD Fabrication, LCD Glass Substrate."**

The TEC member details are as given below:

1. Dr. M. J. Zarabi ( former CMD, SCL Ltd.)
2. Prof. Dhrubes Biswas, IIT Kharagpur
3. Prof. Juzer Vasi, IIT, Mumbai
4. Sh. S.K. Marwaha, Director, DeitY – Co-ordinator
5. Shri Vivek Sharma,Vice President, ST Microelectronics
6. Shri Jaswinder Ahuja, Vice President Cadence

3. The Terms of Reference (TOR) of the Technical Evaluation Committee are as follows:

i) **Name of committee:** Technical Evaluation Committee ( ATMP of Logic Microprocessor, Memory, Chip Components, Discrete Semiconductors, Power Semiconductors, LEDs, LCD Fabrication, LCD Glass Substrate)

ii) **Scope:** The committee will provide recommendation regarding the technology proposed by an applicant and whether the said technology is 'State- of –the –art ' or not as per para 8 of M-SIPS Guidelines.

iii) **Deliverables:** The committee will provide it's advise on the submissions with respect to the scope as defined above , made to the committee by the DeitY .

iv) **Mode of Operation :**

**a.** The normal mode of operation will be decision by way of circulation. The submissions may be circulated to all the committee members. The members may provide their views via email and the decision will be taken by consensus. However, whenever necessary a meeting may be convened.

**b.** The committee may seek additional technical information related to product or technology proposed.

v) **Co-opting** : DeitY may nominate other experts as necessary to the Technical. Committee.

vi) **TA/DA**: TA/DA for members for attending of meetings will be borne by the Department of Electronics & IT as per rules.

vi) **Conflict of Interest:** In the case of conflict of interest, it will be the responsibility of the members to inform the Department and withdraw himself/herself from the committee for that particular issue/case.

(Dr Ajay Kumar)
Joint Secretary to Govt. of India
Tel : 24360160

To:

1. All Committee members

Copy to:

1. All Ministries/Departments of Govt. of India
2. Cabinet Secretariat
3. PMO
4. Planning Commission
5. Comptroller and Auditor General of India
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7. DeitY website